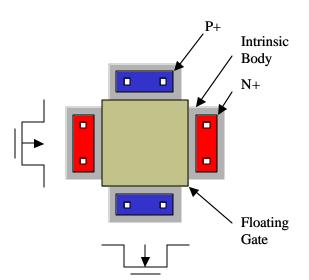
## Radiation Testing of EEPROM Embedded in a Phase Locked Loop M. Burgener, G. Wu, J. W. Swonger, F. Wright, R. Reedy Peregrine Semiconductor

## **Abstract**

EEPROM is widely used in wireless systems for customization of IC functions and storage of system specific data. In this paper we report, for the first time, EEPROM capability embedded in a high performance RF product, including initial radiation testing of the EEPROM cells. The programmable PLL operates to 3 GHz, which requires a high performance RFIC technology. This is the first time EEPROM and its programming circuitry has been integrated into multi-GHz RFIC products. We report the radiation performance of the embedded EEPROM cell, including DC parametrics and programming reliability up to 120 krad, with extrapolated performance to 300 krad

A top view of the EEPROM cell is shown in the figure. It is a unique cell in that it requires no additional mask or processing steps to manufacture. The cell relies of avalanche injection of holes (from the NMOS device) and electrons (from the PMOS device) onto a floating gate. A shared channel and gate enables two states to be stored based on two different polarities of charge. Hence, no control or erase gate is required and over-erase is not possible. This cell is only possible on a fully depleted SOI technology such as Peregrine's UTSi CMOS on sapphire. These features simplify programming, processing and high voltage signal routing, all of which are important to

maintaining a high performance RFIC technology.



Design issues associated with embedding the EEPROM cell into a high performance RF (analog) process without disturbing the core circuit performance will be presented. Issues include embedding the cell; routing the high voltage programming pulses; defining the programming architecture and dealing with ESD when both low and high voltage pulses are required to program the device.

## **Experimental Data**

Pre- and post-irradiation parameters

which will be presented are as follows: EE cell read current; PLL programming reliability supply current (+15V, -15V) (whole board); reference frequency (for purpose of evaluating any post-rad output frequency drift); output VCO frequency; and output power spectrum. The post-radiation data will be extrapolated by comparing the data to design margins; and a method for increasing the radiation hardness will be presented.